WHAT IS CLAIMED IS:

1. A system for multiplexing data onto a SONET/SDH frame, comprising:

a calendar configured to selectively direct input data received from a plurality of channels;

a processor configured to receive the input data and process the input data using virtual concatenation or contiguous concatenation or a combination of both; and

a terminator configured to terminate overhead data within the SONET/SDH frame.

2. The system according to claim 1 wherein the processor is further configured to handle arbitrary virtual concatenation with STS-1 or STS-3c granularity.

3. The system according to claim 1 wherein the processor is further configured to handle contiguous concatenation with STS-Nc capacity, where N is a multiple of 3.

4. The system according to claim 1 wherein the processor is further configured to handle non-standard virtual concatenation and any proprietary concatenation format.

5. The system according to claim 1 wherein the processor is configured to handle mixed concatenation of any contiguous concatenation traffic and virtual concatenation traffic with STS-3c granularity.

6. The system according to claim 1 wherein the system is implemented in a programmable logic device.

7. The system according to claim 1, wherein the processor is further configured to receive and process the overhead data; and the system further comprising:

a shifter configured to redistribute the overhead data and the input data received from the plurality of channels before the overhead data and the input data are selectively directed by the calendar to the processor.

8. The system according to claim 7 wherein the processor is configured to handle any mixed concatenation including STS-1-Xv.

9. The system according to claim 1 wherein the overhead data terminated by the terminator include H1, H2 and H3 bytes in line overhead and H4 byte in path overhead.

10. The system according to claim 9 wherein a multi-frame indicator and a sequence number are inserted into the H4 byte in the path overhead.

11. A system for multiplexing input data from a plurality of channels onto a selected one of a plurality of SONET/SDH frames having different sizes, comprising:

a calendar configured to selectively multiplex the input data received from the plurality of channels;

a processor configured to receive the multiplexed input data and re-arrange the multiplexed input data onto the selected SONET/SDH frame using virtual concatenation or contiguous concatenation or a combination of both; and

a terminator configured to terminate overhead bytes within the selected SONET/SDH frame.

12. The system according to claim 11 wherein the processor further comprises:

an input RAM configured to receive and output the multiplexed input data;

a crossbar configured to receive and re-arrange the multiplexed input data outputted from the input RAM;

an output RAM configured to receive the re-arranged multiplexed data from the crossbar; and

a copy machine configured to control and coordinate operation of the input RAM, the crossbar and the output RAM.

13. The system according to claim 12 wherein the copy machine is further configured to control and coordinate the operation of the input RAM, the crossbar and the output RAM in accordance with a schedule;

wherein the overhead bytes include sequence numbers; and

wherein the calendar, the schedule and the sequence numbers are each double buffered and switched in a predetermined sequence so as to allow hitless re-provisioning.

14. The system according to claim 12 wherein the copy machine is paused when the overhead bytes are inserted into the selected SONET/SDH frame.

15. The system according to claim 12 wherein the input RAM comprises a plurality of memory banks.

16. The system according to claim 12 wherein the input RAM is triple buffered thereby allowing the system to support a fixed latency from data request to data available.

17. The system according to claim 16 wherein the fixed latency is up to N cycles for STS-N traffic.

18. The system according to claim 11 wherein the processor is further configured to handle arbitrary virtual concatenation with STS-1 or STS-3 granularity.

19. The system according to claim 11 wherein the processor is further configured to handle contiguous concatenation with STS-Nc capacity, where N is a multiple of 3.

20. The system according to claim 11 wherein the processor is further configured to handle non-standard virtual concatenation and any proprietary concatenation format.

21. The system according to claim 11 wherein the processor is configured to handle mixed concatenation of any contiguous concatenation traffic and virtual concatenation traffic with STS-3c granularity.

22. The system according to claim 11 wherein the system is implemented in a programmable logic device.

23. The system according to claim 11 wherein the processor is further configured to receive and process the overhead bytes; and the system further comprising:

a shifter configured to redistribute the overhead bytes and the input data received from the plurality of channels before the overhead bytes and the input data are selectively directed by the calendar to the processor.

24. The system according to claim 23 wherein the processor is configured to handle any mixed concatenation including STS-1-Xv.

25. The system according to claim 11 wherein the overhead bytes terminated by the terminator include H1, H2 and H3 bytes in line overhead and H4 byte in path overhead.

26. The system according to claim 25 wherein a multi-frame indicator and a sequence number are inserted into the H4 byte in the path overhead.

27. The system according to claim 11 wherein the different sizes of the plurality of SONET/SDH frames include STS-12, STS-48, STS-192 and STS-768.